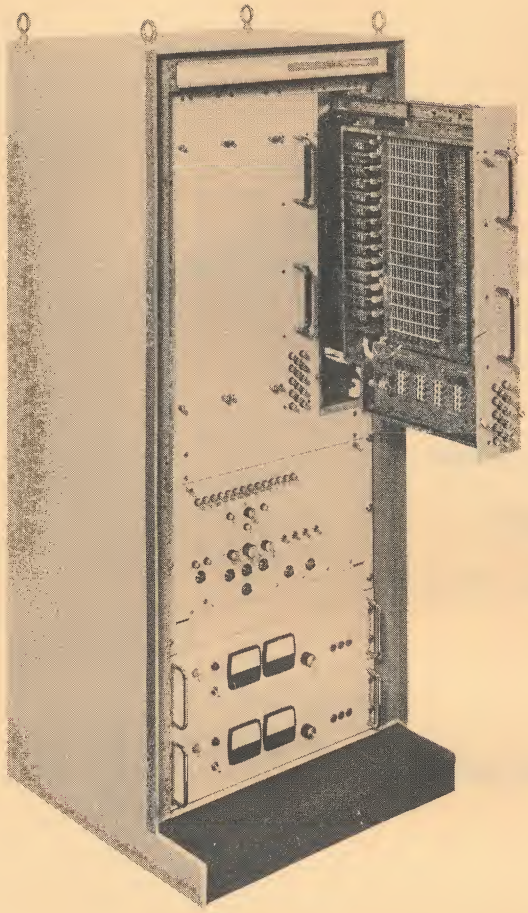
ENGINEERING NOTE

NO. 662

electronic memories inc. 12621 Chadron Avenue • Hawthorne, California 90250 • (213) 772-5201



NANOMEMORY 650™

- 650 nanoseconds cycle time
- High capacity system – up to 16,384 words of 84 bits
- Conservative system timing
- All silicon semiconductors

NANOMEMORY 650™

The NANOMEMORY 650 memory system is an advanced random access, high speed, and high capacity core storage system. Combining 2-1/2D selection techniques with a high speed 20-mil core, a full-cycle time of 650 nanoseconds and access time of 300 nanoseconds is achieved economically, reliably, and with excellent operating margins.

Proven circuits and packaging techniques are used throughout to minimize both propagation delays and "mean-time-to-repair."

In standard configuration, the NANOMEMORY 650 is available in capacities of 4096, 8192, and 16,384 words with word lengths from 8 to 84 bits. Capacities up to 70-bit word length can be installed in 38 inches of a standard 19-inch RETMA rack requiring a depth of only 16 inches (including self-test facilities, but excluding power supplies).

FEATURES

- 20-mil cores
- 2-1/2D selection
- High speed silicon circuitry
- 650 nanoseconds cycle time/300 nanoseconds access time
- Reduced stack and system connections
- Short drive lines
- Capacities up to 16, 384 words of 84 bits
- Five minutes Mean-Time-to-Repair
- Wide operating margins and high reliability
- Compact design
- Low cost per bit
- Circuits compatible with NANOMEMORY 900

INTERFACE SIGNAL FUNCTIONS

The standard NANOMEMORY system uses twisted pair cabling for all signals between processor and memory interface. Single-ended lines are used throughout.

Input Pulses

1. Initiate Pulse – A positive going pulse from the processor commands the start of a cycle.

2. Write 2 Pulse – A positive going pulse from the processor commands the second half (write) of a SPLIT CYCLE operation.

Input Levels

1. Read Mode – A logic level from the processor which, when in the true state, causes the initiate pulse to start a memory READ/RESTORE cycle.

2. Write Mode – A logic level from the processor which, when in the true state, causes the initiate pulse to start a memory CLEAR/WRITE cycle.

3. Split Cycle – A logic level from the processor which, when in the true state, causes the initiate pulse to start the first half of a SPLIT CYCLE operation.

4. Address Input – 8 to 14 single-ended address lines from the processor provide binary coded selection of the required memory storage location.

5. Data Input – 8 to 84 single-ended data lines from the processor provide the binary word which is to be stored during either a CLEAR/WRITE operation or the second half of a SPLIT CYCLE.

Output Pulses

1. Data Available – A single output line from the memory, which indicates the presence of data on the output lines during a READ/RESTORE or SPLIT CYCLE.

2. Optional output pulses for timing purposes can be provided at discrete 25-nanosecond intervals from the beginning of a cycle.

Output Levels

1. Data Output – 8 to 84 single-ended data lines from the memory system carry data to the processor as the result of a READ/RESTORE cycle or first half of a SPLIT CYCLE.

2. Memory Available – A single output line from the memory, when in the true state, indicates that the system may be accessed.

ELECTRICAL CHARACTERISTICS AND TIMING REQUIREMENTS

In its standard form, the NANOMEMORY is supplied with a twisted pair voltage interface. This was selected to provide maximum immunity to ground transients across the memory/processor interface and improve flexibility. However, the interface circuits are such that they can be easily converted to a current interface if required, as a negotiable option.

Input Pulses

The system is triggered by the leading edge of a positive going pulse from the 0 volts nominal level. Nominal pulse amplitude shall be 4.0V ± 1.5V into a line terminating resistor.

Minimum Pulse Width	50 Nanoseconds.
Maximum Pulse Width	500 Nanoseconds.
Maximum Rise Time	40 Nanoseconds.

Pulse widths are measured between 50 percent points.

Input Levels

A logical "1" level is from +2.0V to +5.0V and shall require no current from the drive circuit, exclusive of termination resistor.

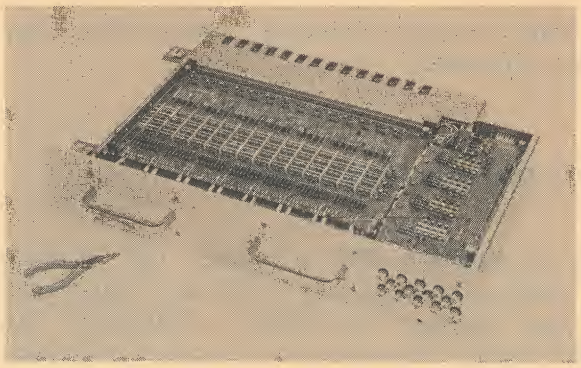
A logical "0" level is from -0.5V to +0.5V and shall source 2.0 ma, exclusive of termination resistor.

Output Pulses

Output pulses are provided through the same type of transmitter circuits as the output levels. Pulse duration shall be 100 nanoseconds nominal.

Output Levels

A logical "1" level is from 3.0V to 3.6V and shall be capable of supplying up to 50 ma current.



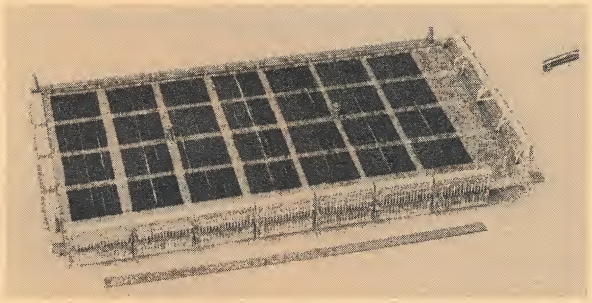
NANOMEMORY 650 Digitized Stack Drawer/Right Side

NANOMEMORY 650
STANDARD FEATURES

1. Self-test facilities and indicator panel.
2. Non-destructive power sequencing.
3. Memory available signal.
4. Automatic register clear at Power On.
5. Pluggable modules throughout.

NANOMEMORY 650
STANDARD OPTIONS

1. Appropriate rack and cabinet.
2. Partial zoning.
3. Register external clear.
4. Timing pulse outputs.
5. Register strobe control.
6. Address register outputs.
7. 200/250 VAC, 50 cps power supply.



NANOMEMORY 650 Magnetics Array (NANOSTAK)™

TECHNICAL SPECIFICATIONS

Capacity	4096, 8192, or 16,384 words. 8 to 70 bits/word in 19-inch rack. 8 to 84 bits/word in 24-inch rack.
Modes of Operation	Clear/Write Read/Restore Split Cycle (Read-modify-write).
Cycle Time	650 nanoseconds Clear/Write or Read/Restore. 775 nanoseconds minimum Split Cycle.
Access Time	300 nanoseconds.
Input Power	115 VAC ± 10 VAC 60 cps. Three wire, single phase.
Power Consumption	See graph.
Operating Environment	
Temperature	+10 to +40°C ambient.
Humidity	Up to 90% RH without condensation.

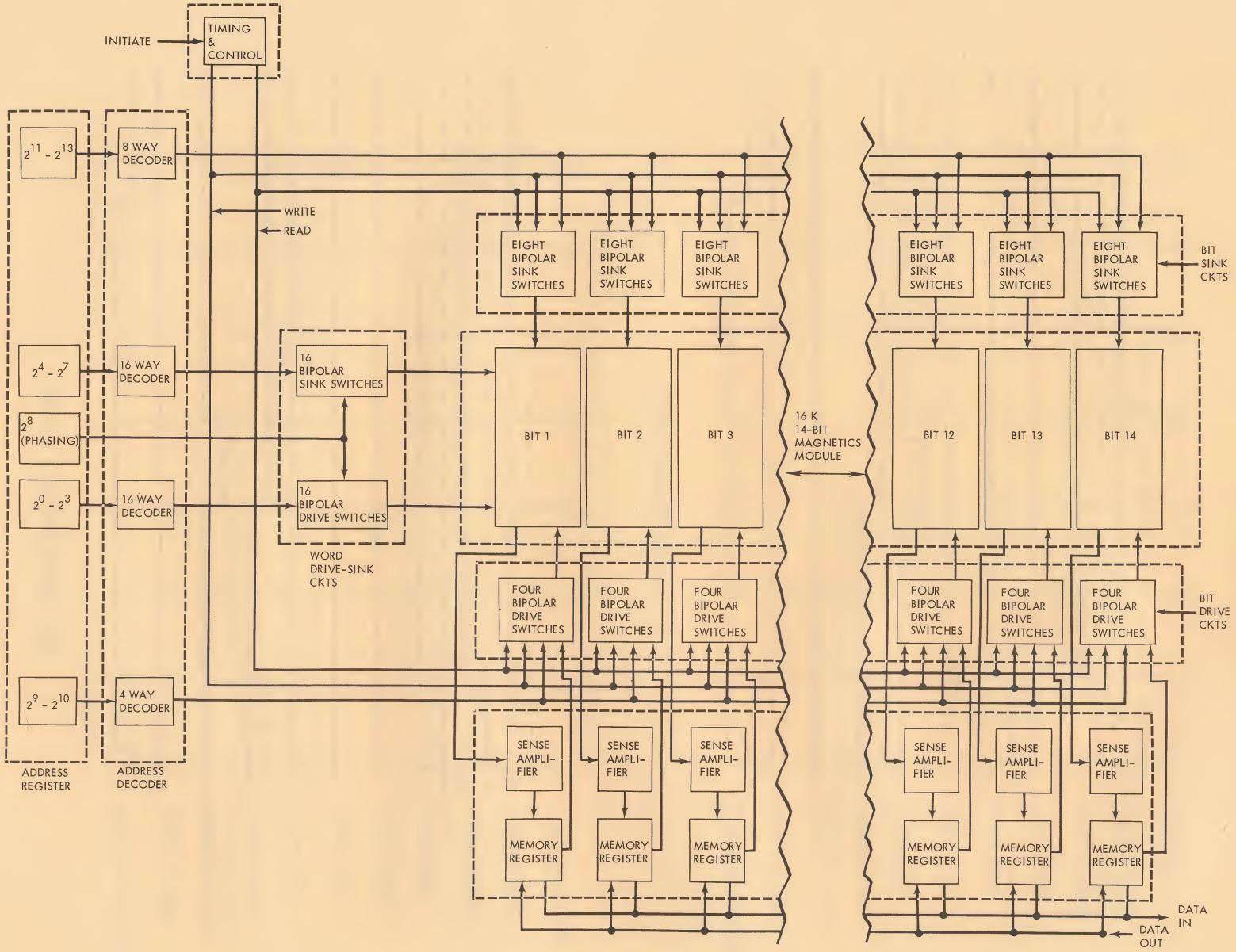
Non-operating Environment	
Temperature	$-40^{o}C$ to $+85^{o}C$.
Humidity	Up to 95% without condensation.
Shock and Vibration	To withstand the shock and vibration of a good commercial shipping environment, when packaged as specified.
Input/Output Interface	Single ended, twisted pair with either voltage or current interface available.
Weight	350 pounds maximum size.

SELF-TEST FACILITY

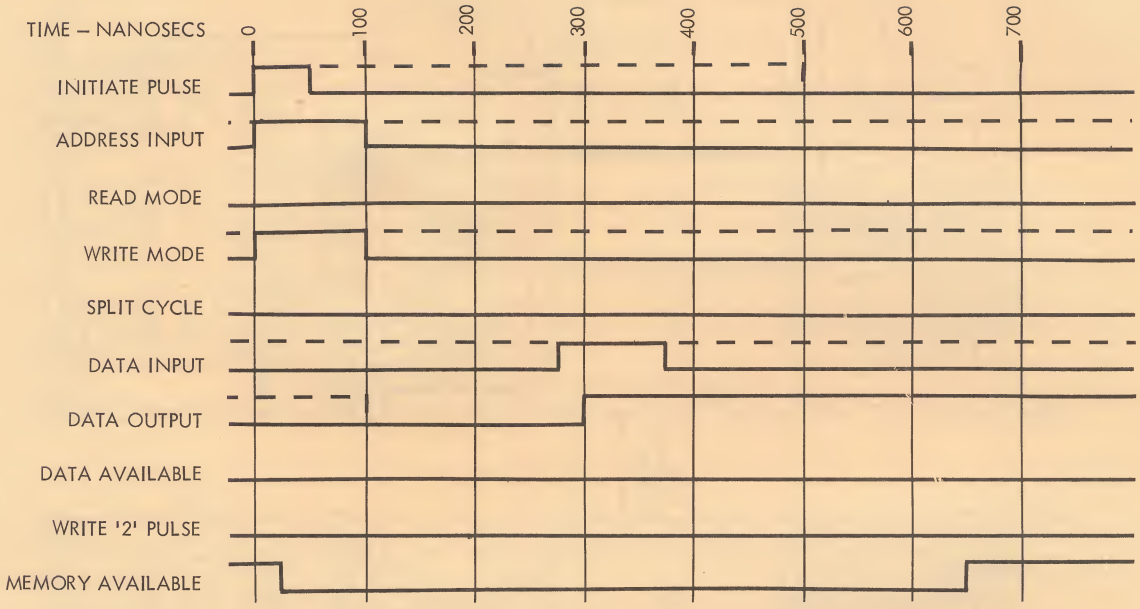
A standard built-in test and indicator system includes generation and checking of the following patterns:

1. All ZEROS.
2. All ONES.
3. WORST CASE PATTERN.
4. WORST CASE PATTERN COMPLEMENT.

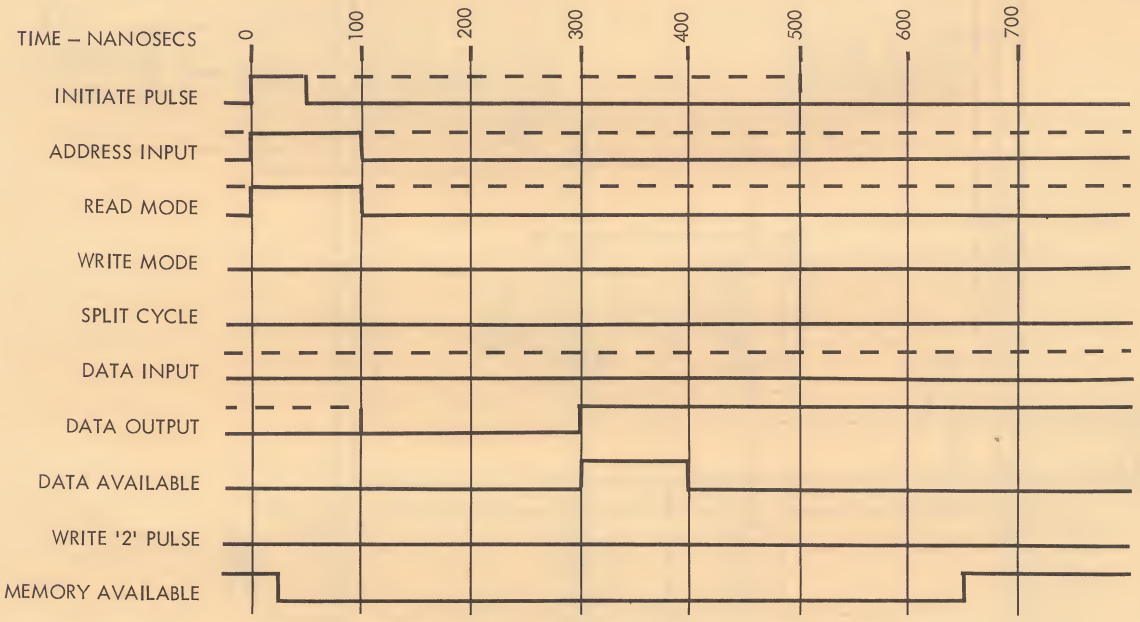
Voltage margin switches are provided to apply discrete ±5% variation on any one or all DC supplies.



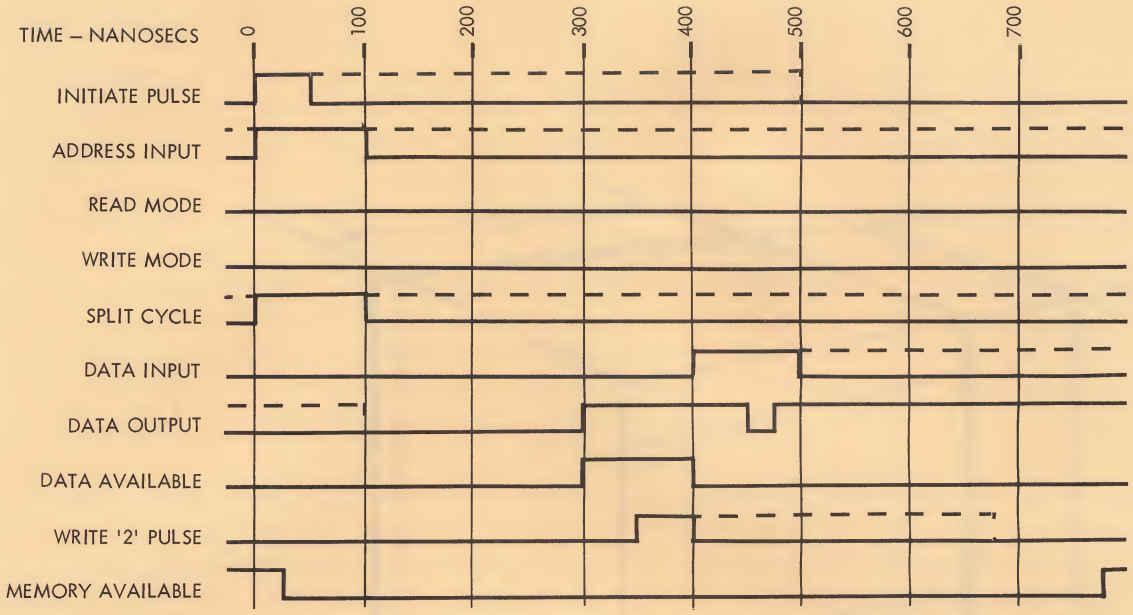
NANOMEMORY 650 Functional Block Diagram



a) Clear/Write Cycle

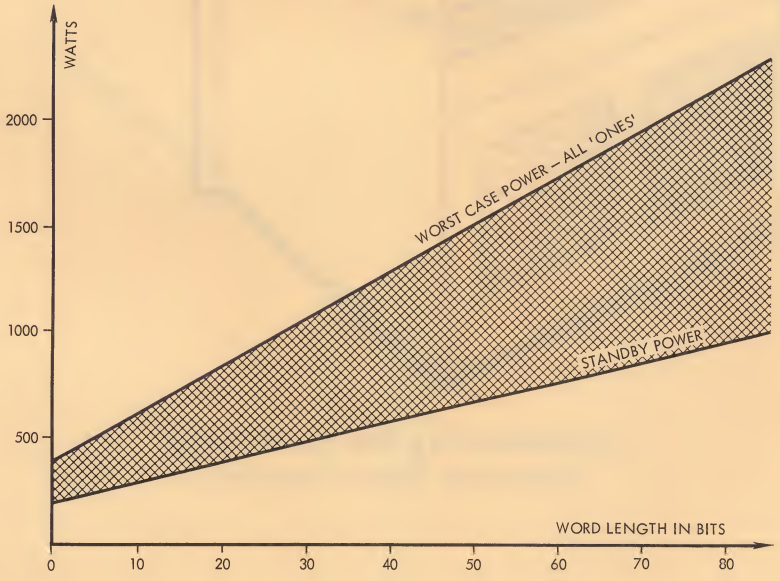


b) Read/Restore Cycle

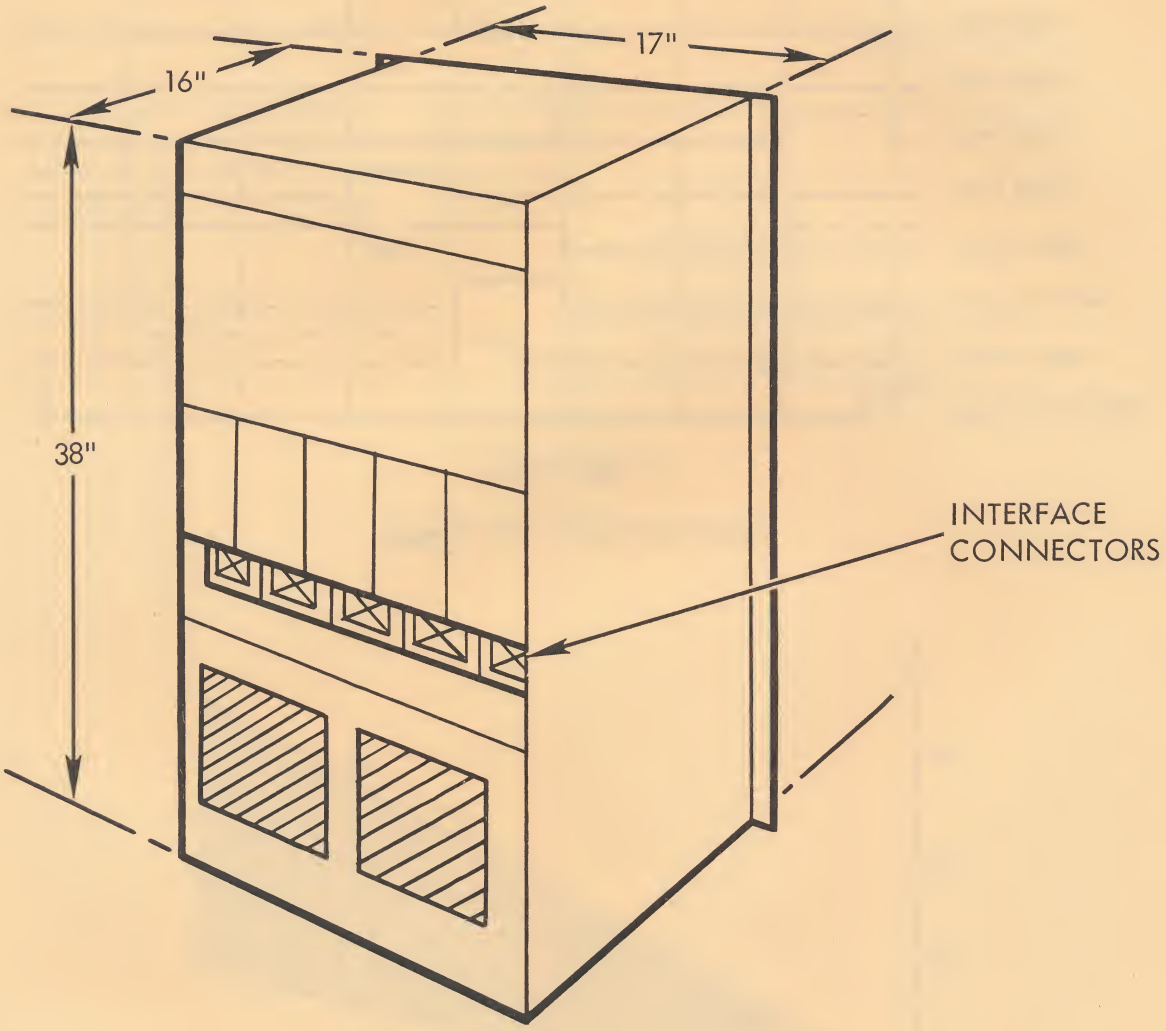


c) Split Cycle

NANOMEMORY 650 Timing



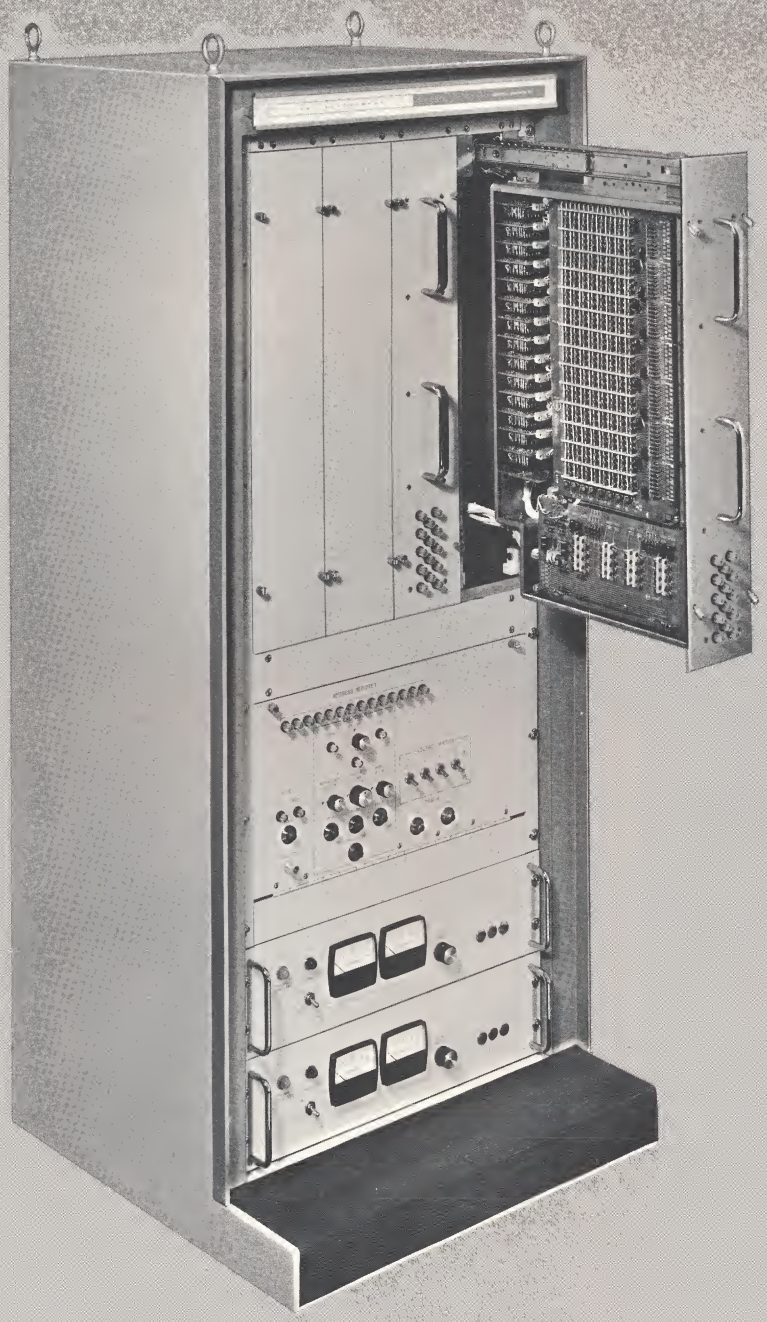
NANOMEMORY 650 Power Consumption



NANOMEMORY 650 Form Factor
(excluding Power Supplies)

Nanomemory™ 900

Commercial Memory System



Nanosecond Megabit Memory

High Speed

Low Cost

High Reliability

Large Capacity

electronic memories inc. 12621 Chadron Avenue, Hawthorne, California 90250, (213) 772-5201

Nanosecond Megabit Memory

The NANOMEMORY 900 is a very high speed and highly reliable memory which uses a new and simple magnetic organization known as 2½D.

The combination of 2½D selection techniques, 30-mil cores and all silicon semiconductors provides:

- ☐ Capacity up to 16,384 words of 84 bits
- ☐ High Speed: 900 nanosecond cycle / 350 nanosecond access time.
- ☐ Reduction of stack connections by a factor of approximately 5 to 1.
- ☐ Compact design.
- ☐ Improved operating margins and system reliability.
- ☐ Simplified DC power requirements.
- ☐ Low cost per bit.

2½D

The NANOMEMORY 900 system pioneers the use of 2½D selection techniques. This new and powerful design combines the advantages of linear select write and coincident current read operations. The economy and equipment reliability previously associated only with slower 30-mil systems is now available at a full cycle time of 900 nanoseconds.

Reliability and Ease of Maintenance

Optimum mechanical design and advanced packaging concepts maintain speed and enhance reliability without diminishing ease of field maintainability. The NANOMEMORY'S all-silicon circuitry is packaged and mounted in a highly compact, but convenient, manner. Coordinated electronic and mechanical design has substantially reduced the total number of individual connections per system, with an appropriate increase in operating reliability.

Mean time to repair has been minimized, enabling any failure to be repaired in less than five minutes by simple replacement of a system module.

Standard Configuration

The NANOMEMORY 900 is available in capacities of 4096, 8192, and 16,384 words with bit lengths from 8 to 84 bits per word. Capacities up to 70-bit word length can be installed in 38 inches of standard 19-inch RETMA rack, requiring a depth of only 16 inches (including self-test facilities, but excluding power supplies).

Interface Signals

The standard NANOMEMORY 900 system uses twisted pair cabling for all signals between processor and memory interface. Single-ended lines are used throughout.

Input Pulses

1. *Initiate Pulse* — A positive going pulse from the processor commands the start of a cycle.
2. *Write 2 Pulse* — A positive going pulse from the processor commands the second half (write) of a SPLIT CYCLE operation.

Input Levels

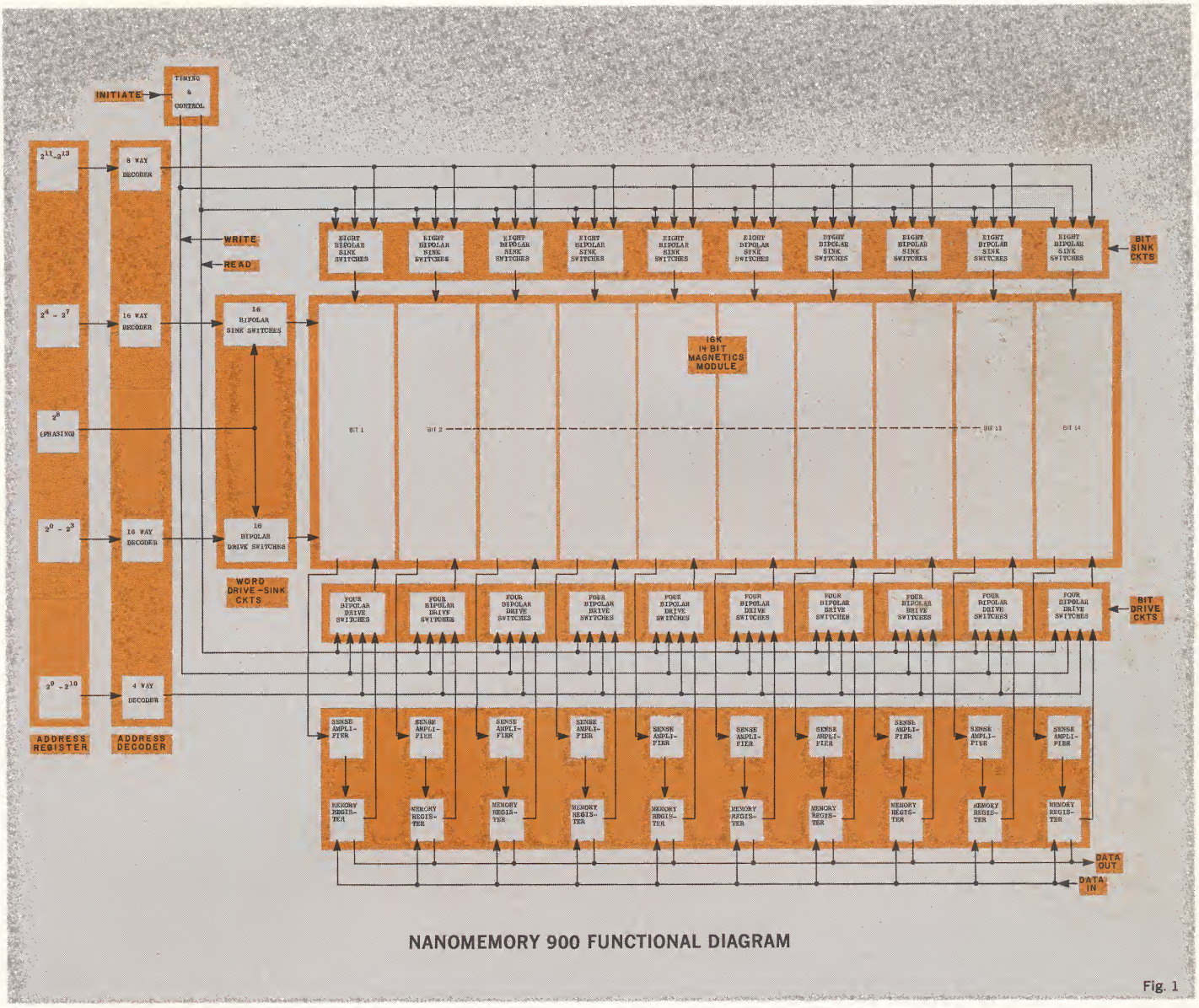
1. *Read Mode* — A logic level from the processor which, when in the true state, causes the initiate pulse to start a memory READ / RESTORE cycle.
2. *Write Mode* — A logic level from the processor which, when in the true state, causes the initiate pulse to start a memory CLEAR / WRITE cycle.
3. *Split Cycle* — A logic level from the processor which, when in the true state, causes the initiate pulse to start the first half of a SPLIT CYCLE operation.
4. *Address Input* — 12 to 14 single-ended address lines from the processor provide binary coded selection of the required memory storage location.
5. *Data Input* — 8 to 84 single-ended data lines from the processor provide the binary word which is to be stored during either a CLEAR / WRITE operation or the second half of a SPLIT CYCLE.

Output Pulses

1. *Data Available* — A single output line from the memory, which indicates the presence of data on the output lines during a READ / RESTORE or SPLIT CYCLE.
2. Optional output pulses for timing purposes can be provided at discrete 25-nanosecond intervals from the beginning of a cycle.

Output Levels

1. *Data Output* — 8 to 84 single-ended data lines from the memory system carry data to the processor as the result of a READ / RESTORE cycle or first half of a SPLIT CYCLE.
2. *Memory Available* — A single output line from the memory, when in the true state, indicates that the system may be accessed.



NANOMEMORY 900 FUNCTIONAL DIAGRAM

Fig. 1

Electrical Characteristics & Timing

In its standard form, the NANOMEMORY 900 is supplied with a twisted pair voltage interface. This was selected to provide maximum immunity to ground transients across the memory/processor interface and improve flexibility. However, the interface circuits are such that they can be easily converted to a current interface if required, as an option.

Input Pulses

The system is triggered by the leading edge of a positive going pulse from the 0 volts nominal level. Nominal pulse amplitude shall be 4.0V ± 1.5V into a line terminating resistor.

Minimum Pulse Width	50 Nanoseconds.
Maximum Pulse Width	500 Nanoseconds.
Maximum Rise Time	40 Nanoseconds.

Pulse widths are measured between 50% points.

Input Levels

A logical "1" level shall be from +2.0V to +5.0V and shall require no current from the drive circuit, exclusive of termination resistor.

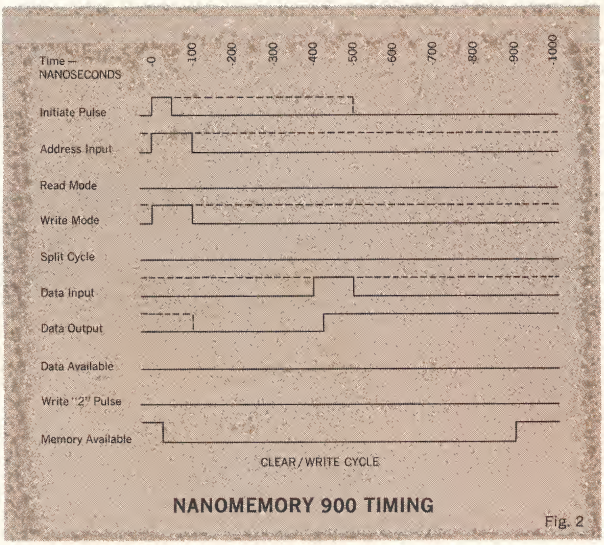
A logical "0" level shall be from −0.5V to +0.5V and shall source 3.5 ma exclusive of termination resistor.

Output Pulses

Output pulses shall be provided through the same type of transmitter circuits as the output levels. Pulse duration shall be 100 nanoseconds nominal.

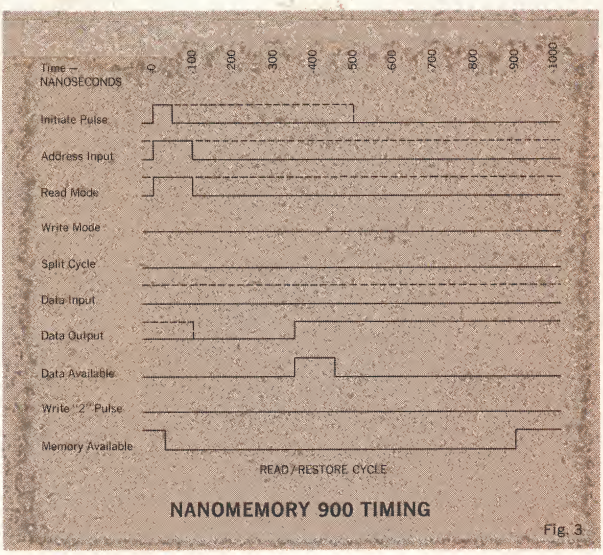
Output Levels

A logical "1" level shall be from +3.6V to +4.2V and shall be capable of supplying up to 50 ma current.



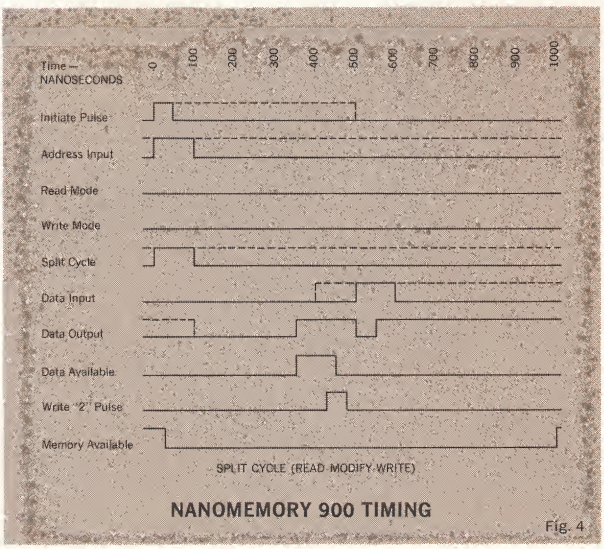
NANOMEMORY 900 TIMING

Fig. 2



NANOMEMORY 900 TIMING

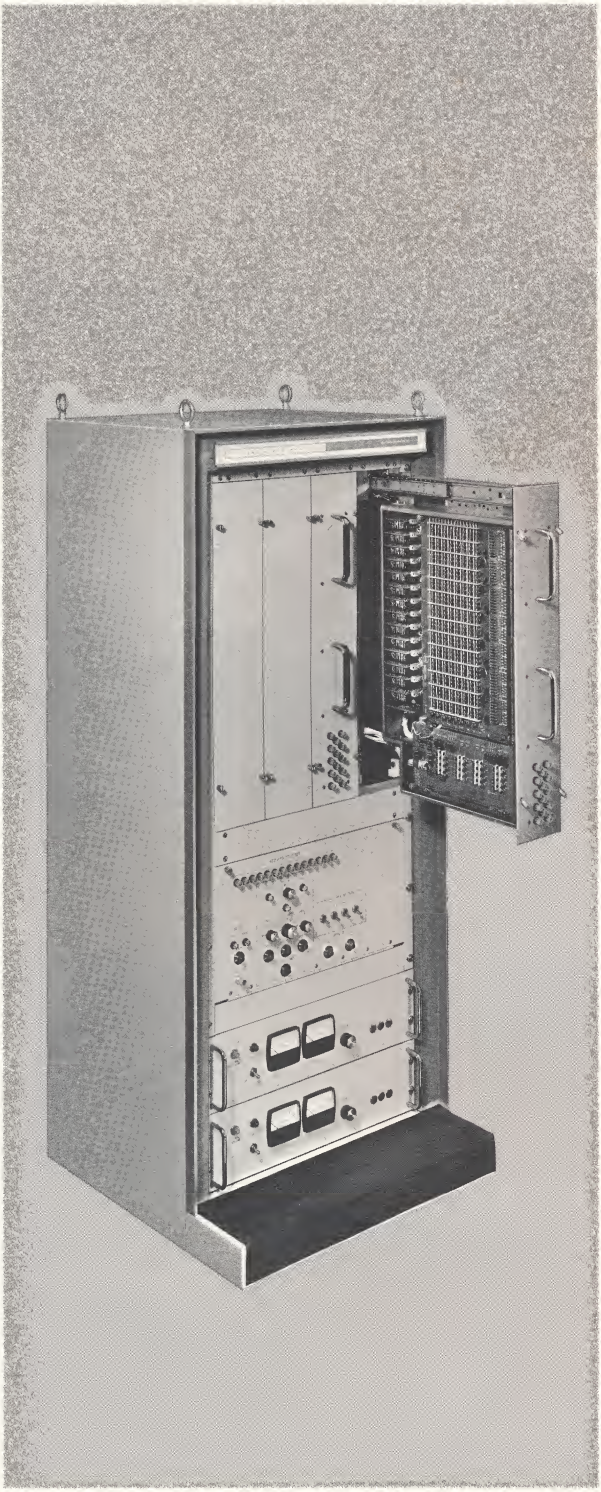
Fig. 3



NANOMEMORY 900 TIMING

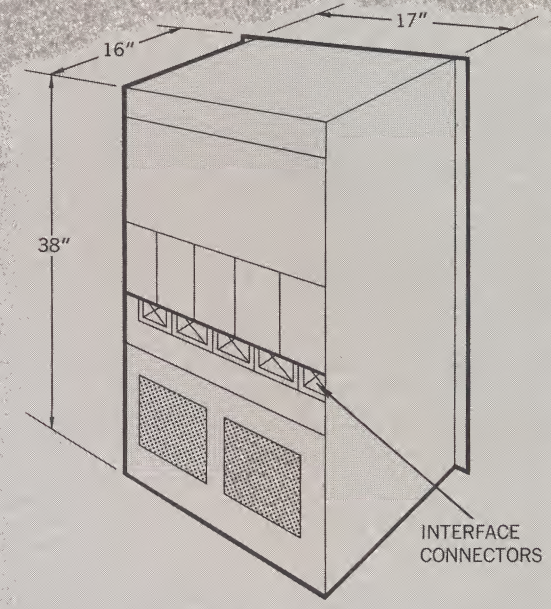
Fig. 4

Nanomemory™ 900



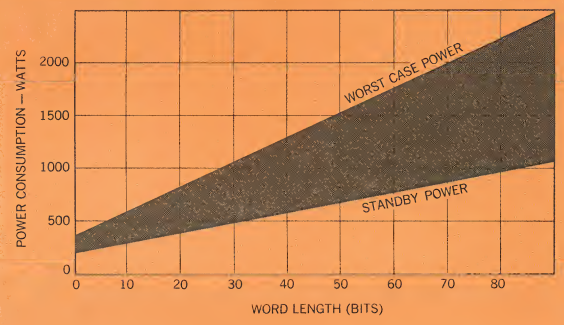
Technical Specifications

Capacity:	4096, 8192 or 16,384 words 8 to 70 bits per word in 19-inch rack 8 to 84 bits per word in 24-inch rack
Modes of Operation:	CLEAR / WRITE READ / RESTORE SPLIT CYCLE
Cycle Time:	900 Nanoseconds CLEAR / WRITE or READ / RESTORE 1000 Nanoseconds minimum SPLIT CYCLE
Access Time:	350 Nanoseconds
Input Power:	115 VAC ±10 VAC, 60 cps. three-wire, single-phase
Power Consumption:	See Figure 6.
Operating Environment:	
Temperature	+10°C to +40°C ambient
Humidity	Up to 90% RH with no condensation
Non-Operating Environment:	
Temperature	−40°C to +85°C
Humidity	Up to 95% with no condensation
Shock & Vibration	To withstand the shock and vibration of a good commercial shipping environment when packaged as specified
Input-Output Interface:	Single-ended, twisted pair
Weight:	350 lbs. maximum size.



NANOMEMORY FORM FACTOR
Excluding Power Supplies

Fig. 5



NANOMEMORY 900, POWER v. WORD LENGTH

Fig. 6

Nanomemory 900 Standard Features

1. Self-Test facilities and indicator panel.
2. Non-destructive power sequencing.
3. Memory available signal.
4. Automatic register clear at Power-on.
5. Pluggable modules throughout.

Nanomemory 900 Standard Options

1. Appropriate rack and cabinet.
2. Partial zoning.
3. Register external clear.
4. Timing pulse outputs.
5. Register strobe control.
6. Address register outputs.
7. 200 / 250 VAC, 50 cps power supply.

Test Feature

A standard built-in self-test and indicator system includes generation and checking of the following patterns:

1. All ZERO's
2. All ONE's
3. Worst-Case Pattern
4. Worst-Case Pattern Complement

Voltage margin switches are provided to apply discrete ±5% variation of all DC supplies.

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